In the Claims:

1. (Currently Amended) A method for manufacturing ~~an integrated circuit comprising~~ a trench structure having sidewalls formed in a depth under the surface of a semiconductor substrate, said method comprising:

providing said semiconductor substrate comprising a crystalline material with a crystal lattice with crystal faces that are more resistant to etching and with crystal faces that are less resistant to etching;

defining at the surface of the semiconductor substrate first areas of a rectangular surface grid having an x axis and a y axis, ~~x axes and a y axes; positioning~~ said x and y axes of the surface grid positioned to be parallel to the crystal faces that are less resistant to etching; [[and]]

etching a surface opening of said trench structures in said first areas; ~~areas,~~ and

etching said sidewalls of ~~said portion of~~ the trench structures formed in a depth under said surface of said semiconductor substrate by etching said crystal faces that are less resistant to etching so as to expand said sidewalls beneath said ~~second~~ first areas of said surface grid.

2. (Previously Presented) The method of claim 21, wherein said surface opening of a trench structure opening is imaged onto the first areas of the surface of the semiconductor substrate by means of an exposure device.

3. (Previously Presented) The method of claim 2, wherein prior to imaging, a mask opening defining rectangular sides in a layout of the trench structure is oriented so that

the rectangular sides are parallel with the crystal faces of the semiconductor substrate that are less resistant to etching.

4. (Currently Amended) The method of claim 21, wherein the semiconductor substrate comprises a semiconductor wafer ~~is provided as the semiconductor substrate and~~ that includes a marking identifying a crystal orientation of the crystal lattice ~~is provided at the semiconductor wafer~~.

5. (Currently Amended) The method of claim 4, wherein the marking identifies ~~a crystal orientation identifying~~ the orientation of the crystal faces that are less resistant to etching ~~is identified by the marking~~.

6. (Original) The method of claim 5, wherein the marking is used for the orientation of a mask in an exposure device.

7. (Currently Amended) The method of claim 21, further comprising etching ~~the~~ an opening at the surface of the semiconductor substrate with an oval cross section.

8. (Currently Amended) The method of claim 21, wherein ~~monocrystalline silicon is provided as the material of~~ the semiconductor substrate comprises monocrystalline silicon.

9. (Original) The method of claim 8, wherein the surface grid is oriented in accordance with a <100> crystal orientation of the monocrystalline silicon.

10. (Currently Amended) The method of claim 9, wherein ~~during the etching process,~~ the <100> crystal faces comprise the crystal faces that are less resistant to ~~having a lower~~ etching ~~resistance are etched more rapidly than~~ and the <110> crystal faces comprise the crystal faces that are more resistant to etching.

11. (Currently Amended) The method of claim 21, further comprising providing ~~wherein~~ upper sections of the trench structures, between the surface of the semiconductor substrate and at least one lower edge of the secondary structures, ~~are provided~~ with a protective layer that is resistant to the etching process that expands said sidewalls of said trench structure.

12. (Previously Presented) The method of claim 21, wherein the trench structures are functionally designed as storage capacitances.

13. (Currently Amended) The method of claim 12 ~~claim 21~~, wherein the secondary structures ~~are~~ comprise selection transistors formed in the second areas for use with the storage capacitances of DRAM cells.

14-20. (Canceled)

21. (Currently Amended) A method for increasing a structure size of trench structures in a depth under a surface of a semiconductor substrate, said method comprising:

providing said semiconductor substrate comprising a crystalline material with a crystal lattice with crystal faces that are more resistant to etching and with crystal faces

that are less resistant to etching;

defining first areas for forming said trench structures in a checker-board fashion in a rectangular surface grid having an ~~x axes and a y axes~~ x axis and a y axis, at a surface of the semiconductor substrate, said first areas alternating with second areas for forming secondary structures in a section of the semiconductor substrate that is near a surface thereof, ~~; positing~~ said ~~x axes and y axes~~ x axis and y axis of the surface grid positioned to be parallel to the crystal faces that are less resistant to etching; and

performing area-selective etching to increase the structure size of the trench structures in said depth under said semiconductor substrate's surface, said structure size of said trench structures expanded along said crystal faces that are less resistant to etching beneath said second areas for forming said secondary structures by said area selective etching.

22. (Previously Presented) The method of claim 1, wherein a trench structure is imaged onto the surface of the semiconductor substrate by means of an exposure device with the x, y axes of the surface grid parallel to the crystal faces of the semiconductor substrate that are less resistant to etching.

23. (Previously Presented) The method of claim 22, wherein prior to said imaging, a mask having rectangular mask openings in a layout of the large structure is oriented such that the sides of the rectangular mask opening are parallel with the crystal faces of the semiconductor substrate that are less resistant to etching.

24. (Currently Amended) The method of claim 1, wherein the semiconductor substrate comprises a semiconductor wafer ~~is provided as the semiconductor substrate and~~ that includes a marking identifying a crystal orientation of the crystal lattice ~~is provided at the semiconductor wafer~~.

25. (Currently Amended) The method of claim 24, wherein the marking identifies ~~said crystal orientation represents~~ the orientation of the crystal faces that are less resistant to etching ~~is identified by the marking~~.

26. (Previously Presented) The method of claim 25, wherein said marking is used for orienting a patterned mask.

27. (Currently Amended) The method of claim 1, wherein ~~further comprising~~ etching a surface opening of the trench ~~structure opening at the surface of the semiconductor substrate~~ comprises etching with an oval cross section.

28. (Currently Amended) A method for manufacturing ~~an integrated circuit comprising~~ a trench structure having sidewalls formed in a depth under the surface of a semiconductor substrate, said method comprising:

providing said semiconductor substrate comprising a crystalline material with a crystal lattice with crystal faces that are more resistant to etching and with crystal faces that are less resistant to etching;

defining at the surface of the semiconductor substrate first areas of a rectangular surface grid having an ~~x axes and a y axes~~ x axis and a y axis, said first areas being located in checker-board fashion for forming said trench structures, said first areas

alternating with second areas of said rectangular surface grid, said second areas being provided for forming secondary structures in a section of the semiconductor substrate that is near said surface thereof, ~~thereof, positioning~~ said x and y axes of the surface grid positioned to be parallel to the crystal faces that are less resistant to etching; and

etching a surface opening of said trench structures in said first areas.

29. (Currently Amended) The method of claim 28, wherein the secondary structures ~~are~~ comprise selection transistors.

30. (Previously Presented) The method of claim 28, wherein a trench structure is imaged onto the surface of the semiconductor substrate by means of an exposure device with the x, y axes of the surface grid parallel to the crystal faces of the semiconductor substrate that are less resistant to etching.

31. (Previously Presented) The method of claim 30, wherein prior to said imaging, a mask having rectangular mask openings in a layout is oriented such that the sides of the rectangular mask opening are parallel with the crystal faces of the semiconductor substrate that are less resistant to etching.

32. (Currently Amended) The method of claim 28, wherein the semiconductor substrate comprises a semiconductor wafer ~~is provided as the semiconductor substrate and~~ having a marking identifying a crystal orientation of the crystal lattice ~~is provided at the semiconductor wafer~~.

33. (Currently Amended) The method of claim 32, wherein the marking identifies ~~said crystal orientation represents~~ the orientation of the crystal faces that are less resistant to etching ~~is identified by the marking~~.

34. (Currently Amended) The method of claim 33, ~~wherein~~ further comprising using said marking ~~is used~~ for orienting a patterned mask.

35. (Currently Amended) The method of claim 28, ~~further comprising~~ wherein etching the ~~trench structure~~ surface opening ~~at the surface of the semiconductor substrate~~ comprises etching with an oval cross section.

36. (New) A method of fabricating a semiconductor device, the method comprising:

providing a silicon substrate having <100> crystal faces and <110> crystal faces;

forming an array of rows and columns of trench structures at a surface of the semiconductor substrate, the rows and columns being parallel to the <100> crystal faces, the etching comprising:

etching the semiconductor substrate to form upper portions of the trench structures;

forming a protective layer over the upper portions of the trench structures; and

etching the semiconductor substrate to form lower portions of the trench structures beneath the upper portions, the lower portions being wider than the upper portions.

37. (New) The method of claim 36, wherein etching the semiconductor substrate to form upper portions of the trench structures comprises forming upper portions that each have a substantially oval shape with long sides oriented parallel to the <100> crystal face.

38. (New) The method of claim 37, wherein etching the semiconductor substrate to form lower portions of the trench structures comprises forming lower portions that each have a substantially rectangular shape with sides parallel to the <110> crystal face.

39. (New) The method of claim 36, further comprising forming a plurality of capacitor, each capacitor being formed in an associated one of the trench structures.

40. (New) The method of claim 39, further comprising a plurality of secondary structures, each secondary structure comprising an access transistor functionally coupled to one of the capacitors.

41. (New) The method of claim 40, wherein the lower portions of the trenches structures extend beneath the secondary structures.

42. (New) The method of claim 36, wherein the semiconductor substrate comprises a semiconductor wafer having a marking identifying a crystal orientation of the crystal lattice.

43. (New) The method of claim 42, wherein the marking identifies the crystal orientation of the <100> crystal faces.

44. (New) The method of claim 43, wherein etching the semiconductor substrate to form upper portions of the trench structures comprises using the marking to orient a patterned mask.